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# UTILITY PATENT APPLICATION TRANSMITTAL

*(Only for new nonprovisional applications under 37 CFR 1 53(b))*

*Attorney Docket No. 0756-2183*

*First Inventor or Application Identifier: Shunpei YAMAZAKI*

*Title: METHOD OF FORMING INSULATING FILMS, CAPACITANCES, AND SEMICONDUCTOR DEVICES*

*Express Mail Label No.*

## APPLICATION ELEMENTS

*See MPEP chapter 600 concerning utility patent application contents*

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification — *Total Pages* [16]
   *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) — *Total Sheets* [4]
4. [X] Oath or Declaration — *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1 63(d))
   *(for continuation/divisional with Box 17 completed)*
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

## ADDRESS TO:

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Washington, DC 20231

6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
   *(when there is an assignee)*
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
    *(if foreign priority is claimed)*
16. [X] Other: Notice of Change of Company Name and Address

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment*
Divisional of prior application Serial No. 08/857,556 filed May 16, 1997; which itself is a Division of Serial No. 08/250,344 filed May 27, 1994, now U.S. Patent 5,665,210; which is a Continuation of Serial No. 08/041,520 filed March 30, 1993, now abandoned; which is a Continuation of Serial No. 07/729,533, filed July 5, 1991, now abandoned.
Prior application information: Examiner: S. Crane Group/Art Unit: 2811

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Signature Date: July 20, 2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re DIVISIONAL Application of | ) |
| Shunpei YAMAZAKI | ) |
| Based On Serial No. 08/857,556 | ) Art Unit: 2811 |
| Which Was Filed: May 16, 1997 | ) Examiner: S. Crane |
| For: METHOD OF FORMING INSULATING | ) |
| FILMS, CAPACITANCES, AND | ) |
| SEMICONDUCTOR DEVICES | )Date: July 20, 2000 |

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Division of Application Serial No. 08/857,556 filed May 16, 1997; which itself is a Division of Serial No. 08/250,344 filed May 27, 1994, now U.S. Patent

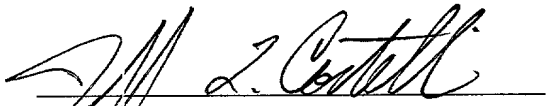
5,665,210; which is a Continuation of Serial No. 08/041,520 filed March 30, 1993, now abandoned; which is a Continuation of Serial No. 07/729,533, filed July 5, 1991, now abandoned.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,



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TITLE OF THE INVENTION

Method of Forming Insulating Films, Capacitances, and Semiconductor Devices

BACKGROUND OF THE INVENTION

The present invention relates to a method of forming insulating films in general. More particularly, it relates to such a method of sputtering suitable for forming excellent dielectric films suitable for use in capacitances.

In the recent years, dielectric (insulating) films deposited by CVD have been utilized to form capacitances for use in integrated semiconductor devices. The employment of CVD makes it possible to deposit dielectric films at low temperatures up to 450°C so that inexpensive substrates such as soda lime glass or borosilicate glass substrates can be used. Similar low temperature deposition can be accomplished also by plasma CVD and sputtering in an atmosphere comprising an inert gas such as argon at a density of 100% to 80%. The use of argon has been known to increase the sputtering yield.

In accordance with experiments of the inventor, it has been found that the number of the interface states occurring between the dielectric film and the underlying electrical active region seriously depends upon the argon density of the sputtering atmosphere. A conspicuous example is the case of dielectric films made of tantalum oxide. In this case, many clusters of tantalum atoms of 5 to 50 Å diameter are formed in the oxide film due to stability of metal tantalum. It has been also found that the argon density significantly influences the difference in flat band voltage from the ideal value which indicates the degradation of the film and reflects the state number of fixed charge and the clusters.

There are other attempts to form dielectric films by the use of photo-CVD. In this case, the underlying surface is less damaged and the density of interface states is as low as 2 x

$10^{10}ev^{-1}cm^{-2}$. On the other hand, the deposition of photo-CVD takes much time to complete due to very slow deposition speed so as not to be utilized for massproduction. Furthermore, the long-term reliability is not sure because of hot-electron effect resulting from hydrogen utilized during deposition.

BRIEF SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method of forming high quality insulating films by deposition at low temperatures suitable for use in capacitances.

It is another object of the present invention to provide a method of forming high quality insulating films having high reliability.

It is a further object of the present invention to provide a method of forming a semiconductor device having high reliability.

Additional objects, advantages and novel features of the present invention will be set forth in the description which follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the present invention. The object and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

To achieve the foregoing and other object, and in accordance with the present invention, as embodied and broadly described herein, a dielectric material or an insulating material is sputtered on a substrate in a particularly appropriate atmosphere. Unlike conventional process, the atmosphere is characterized in that no or small proportion of an inert gas, typically argon, is utilized. The inventors have presumed that the disadvantages of argon atoms include stoichiometric disturbance in the product of sputtering and damage or defects caused by collision of argon ions or argon atoms with the

dielectric film resulting in formation of fixed charge.

In the case of sputtering of a metal oxide such as tantalum oxide, titanium oxide or other suitable oxide dielectric materials and barium titanate, lead titanate or similar ferroelectric materials, the inside of a sputtering apparatus is filled with an oxidizing gas containing an inert gas at 25 vol.% or less, e.g. a mixture of oxygen (100% to 75% in volume) and argon (0% to 25% in volume). Other suitable oxidizing gases include $N_2O$ and $O_3$. Particularly, in the case of $O_2$ or $O_3$, unnecessary atoms are not introduced into the oxide film resulting in few pinholes, little damage to dielectric properties and decreased dispersion in dielectric strength.. $O_3$ tends to be decomposed to yield oxygen radicals which enhance progress of the deposition.. Usually, a bulk of a desired one of these oxides is used as the target of the sputtering. A simple metal such as tantalum can be also used as the target by suitably selecting the sputtering condition as explained in the following detailed description.

In the case of sputtering of nitrides, e.g. insulating nitrides such as silicon nitride and aluminum nitride, or resistive nitrides such as tantalum nitride, titanium nitride or other suitable nitride, the inside of a sputtering apparatus is filled with a nitride compound gas containing an inert gas at 50 vol.% or less, preferably 25 vol.% or less, e.g. a mixture of nitrogen (100 vol.% to 75 vol.%) and argon (0 vol.% to 25 vol.%). Other suitable nitride compound gases include ammonia ($NH_3$). Particularly, when very pure nitrogen such as vaporized from liquid nitrogen is used, unnecessary atoms are not introduced into the nitride film resulting in few pinholes, little damage to dielectric property and small dispersion in dielectric strength.

The quality of insulating films can be furthermore improved by using a halogen which would terminate dangling bonds and neutralize alkali ions inadvertently introduced into the films. In this case, a halogen compound gas is introduced

together with the process gas into the sputtering apparatus at 0.2 to 20 vol%. The halogen compound gases include fluorine compounds such as $NF_3$, $N_2F_4$, HF, chloro-fluoro carbon and $F_2$ and chlorine compounds such as $CCl_4$, $Cl_2$ and HCl. If the halogen is introduced too much, the content of the insulating film might be altered. The concentration of the halogen are limited to 0.01 to 5 atom% in general.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the invention and, together with the description, serve to explain the principles of the invention.

Fig.1(A) is a side view showing a MIS (metal-insulator-semiconductor) device manufactured in accordance with a first embodiment of the present invention.

Fig.1(B) is a graphical diagram for explaining the displacement of the flat band voltage.

Fig.2 is a graphical diagram showing the displacement of the flat band voltage versus the argon proportion to an argon and $O_2$ mixture in the sputtering atmosphere.

Figs.3(A) and 3(B) are side views showing a capacitance manufactured in accordance with a second embodiment of the present invention.

Fig.4 is a graphical diagram showing the dielectric strength versus the argon proportion in the sputtering atmosphere.

Fig.5 is a graphical diagram showing the relative dielectric constant versus the argon proportion in the sputtering atmosphere.

Fig.6 is a cross sectional view showing a DRAM provided with a capacitance manufactured in accordance with the first or second embodiment of the present invention.

Fig.7 is a cross sectional view showing another example of DRAM provided with a capacitance manufactured in accordance

with the first or second embodiment of the present invention.

Fig.8 is a graphical diagram showing the displacement of the flat band voltage versus the argon proportion to an argon and $N_2$ mixture in the sputtering atmosphere.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figs.1(A) and 1(B) and Fig.2, a method of manufacturing an insulating film in accordance with a first embodiment of the present invention will be explained. A substrate 1 made of a single crystalline silicon semiconductor is disposed on a substrate holder in an RF magnetron sputtering apparatus (not shown) in which a target of $Ta_2O_5$ has been mounted on a target holder in advance. After evacuating the inside of the apparatus, a gas is introduced thereinto in order to prepare a suitable atmosphere for gas discharge. The gas comprises argon and an oxidizing gaseous compound such as oxygen. Desirably, the constituent gases have 99.999% or higher purities. A tantalum oxide film 3 (insulating film) is then sputtered on the substrate 1 by causing gas discharge between the target holder and the substrate holder. After completion of deposition, the substrate 1 is removed from the apparatus and coated with a round aluminum electrode 4 having a 1mm diameter by electron beam evaporation.

The characteristics of such insulating film in the MIS structure (Al-$Ta_2O_5$-Si) can be evaluated by displacement $\Delta V_{FB}$ of the flat band voltage through measuring the flat band voltage. For the measurement of the displacement, the insulating film is given BT (bias-temperature) treatment with a negative bias voltage of 2 x $10^6$V/cm at 150°C for 30 minutes followed by measuring the flat band voltage $V_{FB1}$, and thereafter BT treatment with a positive bias voltage of 2 x $10^6$V/cm at 150°C for 30 minutes followed by measuring the flat band voltage $V_{FB2}$ again. The displacement $\Delta V_{FB}$ is $|V_{FB1}-V_{FB2}|$ as illustrated in Fig.1(B).

The above procedure of deposition was repeated by changing the proportion of argon to oxygen from 100% to 0% for

reference. The displacements $\Delta V_{FB}$ measured are plotted on a graphical diagram shown in Fig.2. As shown in the diagram, the displacements $\Delta V_{FB}$ significantly decreased below 5 V when the argon proportion was decreased to 25% or lower. When argon was not used, i.e. pure oxygen (100%) was used, the displacements $\Delta V_{FB}$ was only 0.5V or lower. Contrary to this, when pure argon (100%) was used, the displacements $\Delta V_{FB}$ was increased to 10V. The displacements $\Delta V_{FB}$ was furthermore abruptly decreased to several tenths thereof by utilizing an additive of a halogen. The introduction of a halogen is carried out by introducing into the sputtering apparatus, together with oxygen, a halogen compound gas such as a nitrogen fluoride ($NF_3$, $N_2F_4$) at 0.2 to 20 vol%. Particularly, $NF_3$ is most preferred because $NF_3$ can be handled with a little care and decomposed by small energy.

Referring next to Fig.3, a method of manufacturing an insulating film in accordance with a second embodiment of the present invention will be explained. A substrate 1 comprising a sodalime glass plate and a $SiO_2$ blocking film formed thereon is disposed in a sputtering apparatus in which a target of metal tantalum has been set up in advance. After evacuating the inside of the apparatus, a gas is introduced thereinto for gas discharge. The gas comprises argon. A tantalum film 2 in the form of an island (lower electrode) is sputtered on the substrate to a thickness of 2000 Å on the substrate 1 with the aid of a metallic mask by causing gas discharge between the target holder and the substrate holder. Alternatively, a known photolithography may be utilized instead of the use of the metallic mask. The substrate temperature is 350°C. The pressure of the gas is maintained at 0.06 Torr during deposition. The input Rf energy is 100W at 13.56 MHz.

After completion of deposition of the lower electrode 2, the gas is replaced by a mixture of oxygen (100 vol% to 0 vol%) and argon (0 vol% to 100 vol%). The Ta target is also replaced by a $Ta_2O_5$ target having a 99.99% or higher purity. A tantalum oxide

film 3 (insulating film) is then deposited on the lower electrode 2 by sputtering associated with gas discharge between the target holder and the substrate holder. The substrate temperature is 100°C. The pressure of the gas is maintained at 0.05 Torr during deposition. The input Rf energy is 500W at 13.56 MHz. The distance between the substrate 1 and the target is adjusted to be 150mm. After completion of deposition, the substrate 1 is removed from the apparatus and coated with around aluminum film 4 (upper electrode) having a 1mm diameter by electron beam evaporation in order to form a capacitance comprising the lower and upper electrodes 2 and 4 and the interposed insulating (dielectric) film 3.

The characteristics of such a capacitance were also evaluated by measuring the displacement $\Delta V_{FB}$ of the flat band voltage. When 100% oxygen was used, a very excellent capacitance was formed. Even if argon was used up to 25%, capacitances having equivalent qualities were formed by setting the distance between the substrate 1 and the target to be larger than the appropriate value for the case of deposition using pure oxygen. Accordingly, excellent capacitances can be formed by utilizing a mixture of oxygen (100 vol% to 25 vol%) and argon (0 vol% to 75 vol%). The quality of such insulating films can be furthermore improved by introducing a halogen in the same manner as explained in conjunction with the first embodiment. In this case, the introduced halogen atoms can be activated by flash annealing using excimer laser pulses so that dangling bonds occurring in the film are neutralized by the halogen atoms and the origin of fixed charge in the film is eliminated.

Fig.4 is a graphical diagram showing the relationship between the dielectric strength of the film 3 and the oxygen proportion to the argon-oxygen mixture. The dielectric strength is measured as the threshold voltage when the current leakage exceeds 1 μA. In this diagram, the length of vertical lines corresponds to double the standard deviations $\sigma(X)$ and given

center dots indicative of averages respectively. As shown in the diagram, the $\sigma(X)$ decreased and the average dielectric strengths increased as the proportion increased beyond 75%. Fig.5 is a graphical diagram showing the relationship between the relative dielectric constant of the film 3 and the oxygen proportion to the argon-oxygen mixture in the same manner. In this diagram, it is also understood that high proportions of oxygen are advantageous resulting in small dispersions.

Referring next to Fig.6, a suitable application of the insulating film formed in accordance with the first or second embodiment of the present invention will be explained. The insulating film is used to form storage capacitances coupled with gate insulated field effect transistors for constructing a DRAM (dynamic random access memory) of 1 Tr/Cell type.

A storage element of the DRAM is of a stacked type as illustrated in Fig.6 and comprises an n-type silicon semiconductor substrate within which a source and drain regions 8 and 9 of p-type are formed in order to define a channel region therebetween, a field insulating film 5 (LOCOS) for insulating the element from adjacent elements, a gate electrode 7 formed on the channel region through a gate insulating film 6 formed by thermal oxidation or sputtering of silicon oxide in 100% oxygen, an interlayer insulation film 14, a lower electrode 10 made of a silicon semiconductor heavily doped with phosphorus, a dielectric (insulating) film 11 and an upper electrode 12 formed of an aluminum film or a dual film comprising an aluminum layer and a tantalum layer.

The lower electrode 10 may be formed of metal tantalum, tungsten, titanium, molybdenum or any of silicides of such metals and makes electric contact with the drain region 9 through an opening formed in the interlayer film 14. The dielectric film 11 is formed of a $Ta_2O_5$ film deposited by sputtering to a thickness of 300 Å to 3000 Å, typically 500 Å to 1500 Å, e.g. 1000 Å in accordance with the first or second embodiment as described

above. The gate insulating film 6 can be made also from $Ta_2O_5$ in place of silicon oxide. In that case, the number of interface states is as small as 2 x $10^{10}cm^{-2}$. A storage capacitance is formed of the upper and lower electrodes 10 and 12 and the dielectric film 11 located therebetween. The formation of trapping centers of hot carriers can be avoided by forming these electrodes 10 and 12 and the dielectric film 11 in an atmosphere which has been deprived of hydrogen, which otherwise could reach to the gate insulating film by drifting (diffusion). The channel length of the element is selected between 0.1 μm and 1.0 μm, e.g. 0.5 μm so that one storage element can be formed within an area of 20 μm square. The source region 8 is connected to a bit line for example, and in that case the gate electrode 7 is connected to an address line of the memory. Such miniaturized structure becomes possible due to the large storage capacitance originating from the large relative dielectric constant (=27) of the tantalum oxide film as compared to the relative dielectric constant (=3.8) of silicon oxide. The large relative dielectric constant makes it possible to increase the thickness of the dielectric film to, e.g. 1000 Å so that electric insulation is improved and the number of pinholes is decreased. The frequency property of the tantalum oxide film is also excellent and maintained even at high frequencies. In the figure, numeral 12' designates an extension of the upper electrode of an adjacent storage element. Numeral 13 is the bit line of an adjacent element.

Referring next to Fig.7, another application of the insulating film formed in accordance with the first or second embodiment of the present invention will be explained. The insulating film is used to form storage capacitances for a DRAM (dynamic random access memory) of 1 Tr/Cell type.

A storage unit element of the DRAM illustrated in Fig.7 can store information of two bits. The element comprises a p-type silicon semiconductor substrate within which a pair of channel regions 15 and 15' of n-type and a pair of drain regions 8 and 8'

of p-type are formed, a plateau of a p-type semiconductor material forming a source region 9 located between the channel regions 15 and 15', a source electrode 19 formed on the plateau, a pair of gate electrodes 7 and 7' formed on the channel regions 15 and 15' through a gate insulating film 6 and flanking the side surface of the source region 9, a field insulating film 5 (LOCOS) for insulating the element from adjacent elements, an interlayer insulation film 14, a pair of lower electrodes 10 and 10' made of silicon semiconductor heavily doped with phosphorus, a dielectric (insulating) film 11 and a pair of upper electrodes 12 and 12' formed of an aluminum film or a dual film comprising an aluminum layer and a tantalum layer. The channel regions 15 and 15' are formed by ion implantation of boron with a mask of the plateau 9 and 19 and the field insulating film 5 to a density of 1 x $10^{15}$ $cm^{-3}$ to 5 x $10^{16}$ $cm^{-3}$, in advance of the formation of the gate electrodes 7 and 7', followed by ion implantation of phosphorus into the regions 8 and 8' with a mask of the plateau 9 and 19, the field insulating film 5 and the gate electrodes 7 and 7' to a density of 1 x $10^{19}$ $cm^{-3}$ to 1 x $10^{21}$ $cm^{-3}$.

The lower electrodes 10 and 10' make electric contact with the drain regions 8' and 8 through openings formed in the interlayer film 14 respectively. The dielectric film 11 is formed of a $Ta_2O_5$ film deposited by sputtering to a thickness of 300 Å to 3000 Å, typically 500 Å to 1500 Å, e.g. 1000 Å in accordance with the first or second embodiment as described above in the same manner as that of the previous application. The lower electrode may be formed of metal tantalum, tungsten, titanium, molybdenum or any of silicides of these metals in place of the doped silicon semiconductor. A pair of storage capacitances 21 and 21' are formed from the upper and lower electrodes 10, 10' and 12, 12' and the dielectric film 11 therebetween. The channel length of the element is selected between 0.1 μm and 1.0 μm, e.g. 0.5 μm so that a two bit storage element can be formed within an area of 10 to 20 μm square.

Next, a method of manufacturing an insulating film in accordance with a third embodiment of the present invention will be explained. Fig.1(A) is used again for this purpose. A substrate 1 made of a single crystalline silicon semiconductor is disposed on a substrate holder in an RF magnetron sputtering apparatus (not shown) in which a target of $Si_3N_4$ has been mounted on a target holder in advance. Alternatively, the target may be made of other nitrides such as aluminum nitride, tantalum nitride, titanium nitride instead of the $Si_3N_4$ target. After evacuating the inside of the apparatus, a gas is introduced thereinto in order to prepare a suitable atmosphere for gas discharge. The gas comprises argon and a nitrogen compound gas such as nitrogen. Desirably, the constituent gases have 99.9% or higher purities. The substrate temperature is 200°C. The pressure of the gas is maintained at 0.05 Torr during deposition. The input Rf energy is 500W at 13.56 MHz. The distance between the substrate 1 and the target is adjusted to be 150mm. A silicon nitride film 3 (insulating film) is then sputtered on the substrate 1 by causing gas discharge between the target holder and the substrate holder. After completion of deposition, the substrate 1 is removed from the apparatus and coated with a round aluminum electrode 4 having a 1mm diameter by electron beam evaporation.

The characteristics of such insulating film in the MIS structure (Al-$Si_3N_4$-Si) can be evaluated by displacement $\Delta V_{FB}$ of the flat band voltage through measuring the flat band voltage. For the measurement of the displacement, the insulating film is given BT (bias-temperature) treatment with a negative bias voltage of 2 x $10^6$V/cm at 150°C for 30 minutes followed by measuring the flat band voltage, and thereafter BT treatment with a positive bias voltage of 2 x $10^6$V/cm at 150°C for 30 minutes followed by measuring the flat band voltage again in the same manner as for oxide films.

The above procedure of deposition was repeated by

changing the proportion of argon to nitrogen from 100% to 0% for reference. The displacements $\Delta V_{FB}$ measured are plotted on a graphical diagram shown in Fig.8. As shown in the diagram, the displacements $\Delta V_{FB}$ significantly decreased below 2 V when the argon proportion was decreased to 25% or lower. Numeral 31 designates a displacement of 11.5V in the case of a silicon nitride film deposited by a conventional plasma CVD for reference. When argon was not used, i.e. pure nitrogen (100%) was used, the displacements $\Delta V_{FB}$ was only 0.5V or lower as depicted by numeral 34. Contrary to this, when pure argon (100%) was used, the displacements $\Delta V_{FB}$ was increased to 13V. The displacements $\Delta V_{FB}$ was furthermore abruptly decreased to several tenths thereof by utilizing an additive of a halogen. The introduction of a halogen is carried out by introducing into the sputtering apparatus, together with nitrogen, a halogen compound gas such as a nitrogen fluoride ($NF_3$, $N_2F_4$) at 0.2 to 20 vol%. In this case, the introduced halogen atoms can be activated by flash annealing using excimer laser pulses so that dangling bonds occurring in the film are neutralized by the halogen atoms and the origin of fixed charge in the film is eliminated.

Referring again to Figs.6 and 7, suitable applications of the insulating film formed in accordance with the third embodiment of the present invention will be explained. The insulating film is used also in this case to form storage capacitances for DRAMs (dynamic random access memory) of 1 Tr/Cell type. The explanation is substantially same as given to the above applications utilizing the tantalum oxide insulating films except for the following description.

The dielectric film 11 as illustrated in Figs.6 and 7 is formed of a $Si_3N_4$ film in this case deposited by sputtering to a thickness of 300 Å to 3000 Å, typically 500 Å to 1500 Å, e.g. 1000 Å in accordance with the third embodiment as described above. The gate insulating film 6 can be made also from $Si_3N_4$ in place of silicon oxide. In that case, the number of interface

states is as small as 3 x $10^{10}cm^{-2}$. The dimension of the unit elements can be decreased in the same manner as in the applications utilizing the tantalum oxide films due to the large storage capacitance originating from the large relative dielectric constant (=6) of the silicon nitride film as compared to the relative dielectric constant (=3.8) of silicon oxide.

The foregoing description of preferred embodiments has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and obviously many modifications and variations are possible in light of the above teaching. The embodiment was chosen in order to explain most clearly the principles of the invention and its practical application thereby to enable others in the art to utilize most effectively the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

Although the dielectric films are deposited by RF magnetron sputtering in the above preferred embodiments, other suitable sputtering can be utilized, e.g. various known types of DC or RF sputtering methods. It is partly because of the high resistance of the targets utilized that RF magnetron sputtering is preferred. Pure metals such as tantalum and titanium, however, may be used in suitable sputtering conditions. In the case of deposition of oxide films by the use of such targets of pure metals, the atmosphere is purified to a 99.999% or higher purity and comprises 100% to 90% oxygen in which deposition of the oxide films is carried out with a lower acceleration voltage at a lower deposition speed of the order of 1/4 of the above embodiments.

The application of the present invention is not limited to the above examples but applicable for integrated circuits utilizing the capacitors of the present invention, transistors of inversed-stagger type, vertical channel transistors, other types of insulated gate field effect transistors formed within a single crystalline silicon semiconductor substrate and so forth. The

capacitances can be formed into multi-layered structure or vertical type structure in which the dielectric film is sandwiched by a pair of electrodes in a lateral direction. The capacitors of the present invention can be used for dynamic memories.

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a pair of field effect transistors associated with said semiconductor substrate wherein each source of said transistors shares a common impurity doped region formed in a plateau elevated from said semiconductor substrate and each gate electrode of said transistors is formed over each channel region of said transistors;

a first capacitor connected to a drain of one of said transistors;

a second capacitor connected to a drain of another one of said transistors,

wherein said each of said first and second capacitors comprises a pair of electrodes and a dielectric layer interposed therebetween, said dielectric layer comprising a ferroelectric material, and

wherein each of said first and second capacitors is located over said gate electrode of the corresponding transistor so as to completely overlap said gate electrode.

ABSTRACT OF THE DISCLOSURE

Insulating metal oxide or nitride films are deposited by RF magnetron sputtering. During sputtering, the atmospheric gas comprises an oxygen or nitride compound gas and an inert gas. The proportion of the inert gas is decreased to 25 atom% or lower. By this sputtering condition, adverse effects caused by the inert gas is suppressed so that the quality of the insulating film is substantially improved.

FIG. 1A

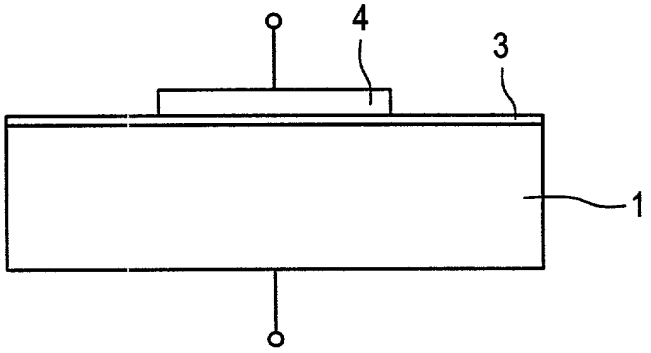



FIG. 1B

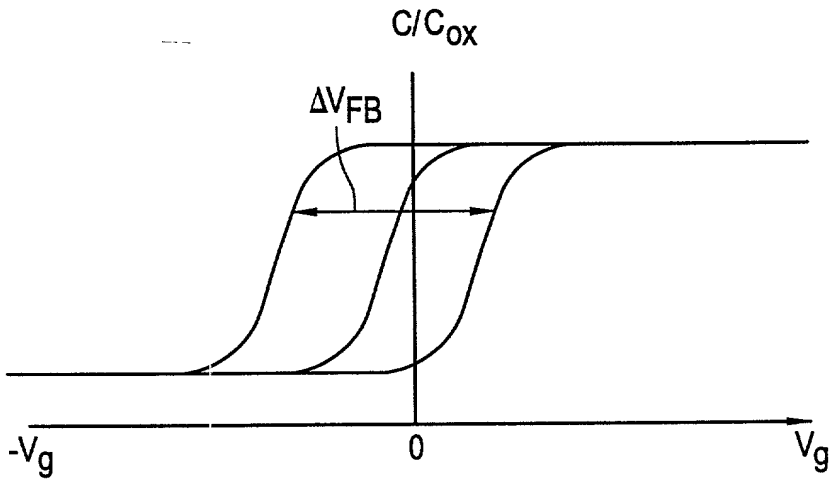


FIG. 2

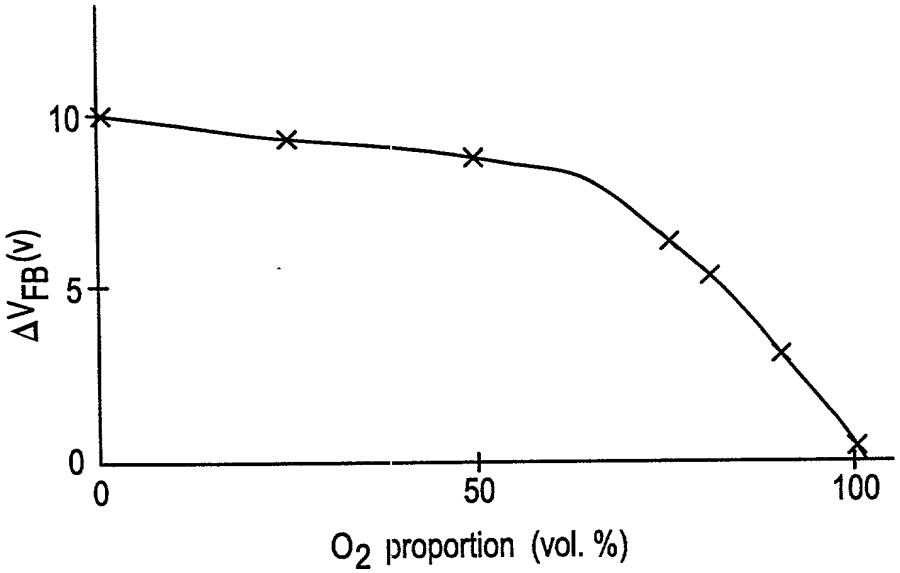



FIG. 3A

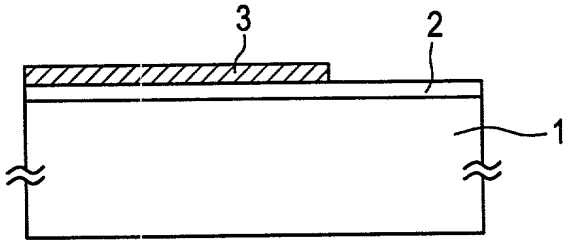



FIG. 3B

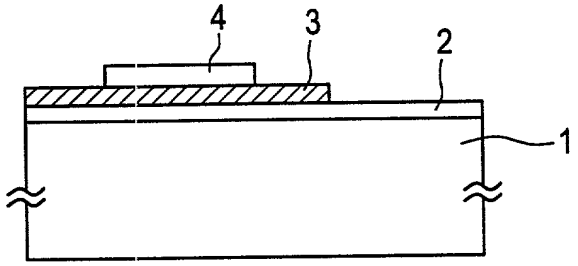


FIG. 4

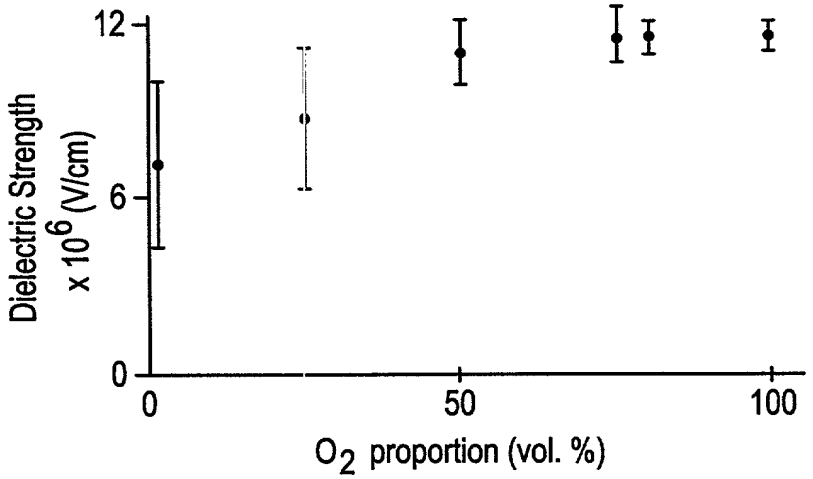



FIG. 5

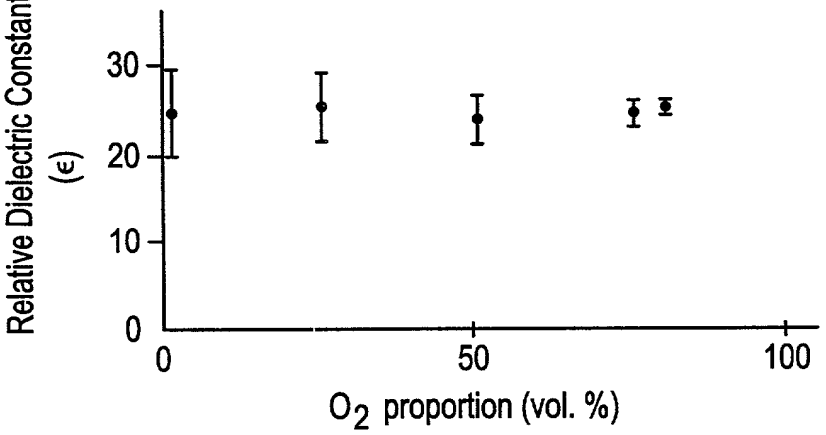



FIG. 8

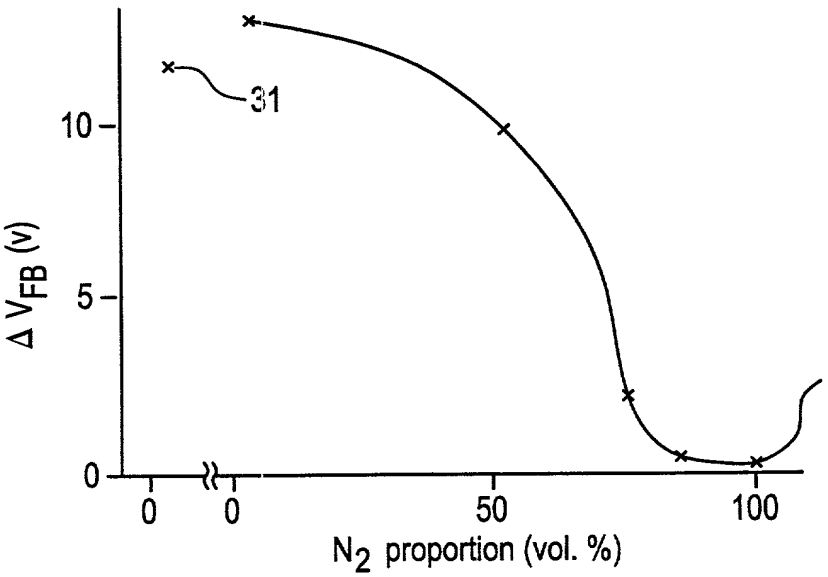
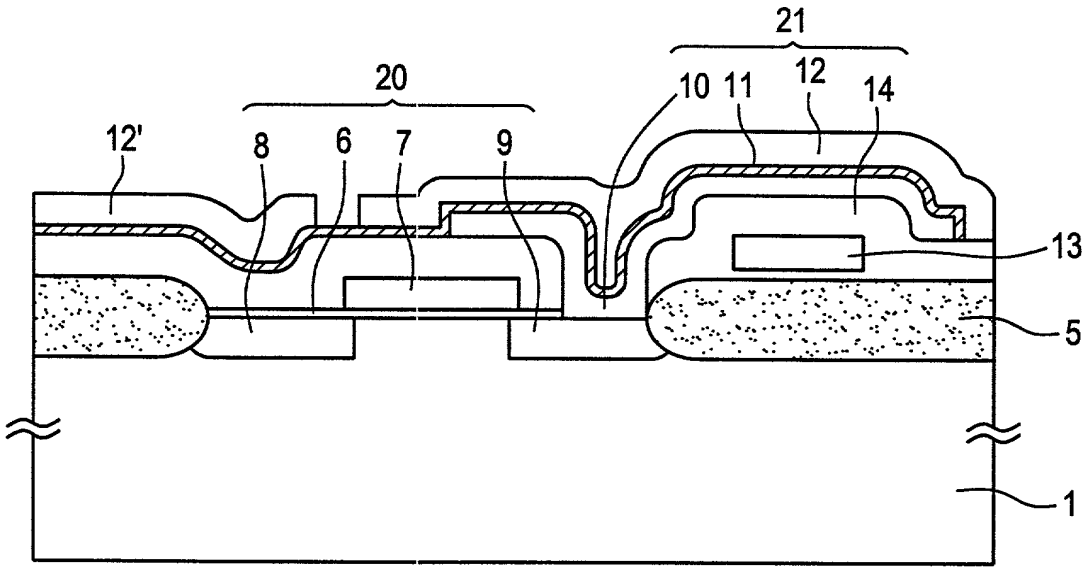


FIG. 6


21
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12'
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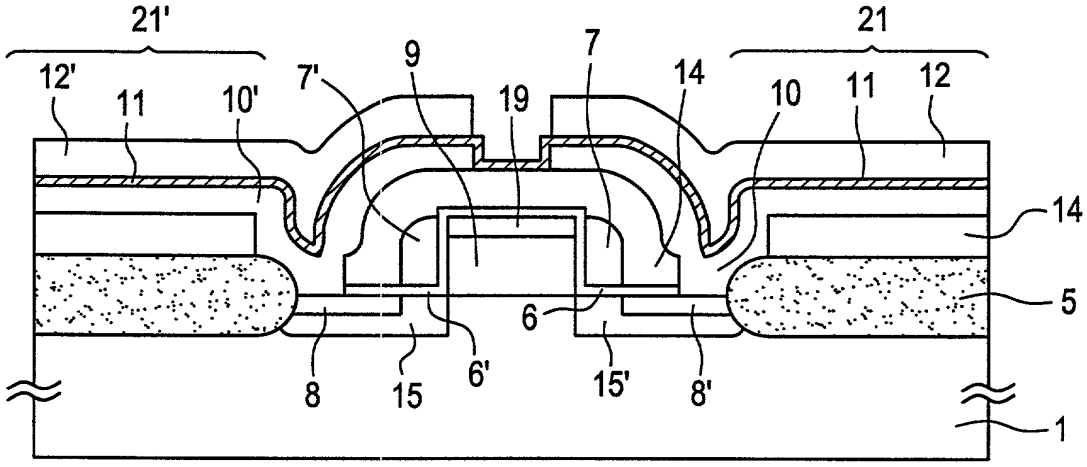
5
1

FIG. 7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12'
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7'
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14
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14
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15
6'
15'
8'
1

# DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * Method of Forming Insulating Films, Capacitances, and Semiconductor Devices, the specification of which is attached hereto unless the following box is checked:

Insert Title

Check Box If Appropriate — For Use Without Specification Attached

☐ The specification was filed on _____
and was assigned Serial No. _____ (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Insert Priority Information (if appropriate)

| Prior Foreign Application(s) | | | Priority Claimed | |
|---|---|---|---|---|
| 2-195174 (Number) | Japan (Country) | July 24, 1990 (Month/Day/Year Filed) | ☒ Yes | ☐ No |
| 2-195175 (Number) | Japan (Country) | July 24, 1990 (Month/Day/Year Filed) | ☒ Yes | ☐ No |
| 2-195176 (Number) | Japan (Country) | July 24, 1990 (Month/Day/Year Filed) | ☒ Yes | ☐ No |
| (Number) | (Country) | (Month/Day/Year Filed) | ☐ Yes | ☐ No |
| (Number) | (Country) | (Month/Day/Year Filed) | ☐ Yes | ☐ No |

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

| Country | Application No. | Date of Filing (Month/Day/Year) |
|---|---|---|
| | | |
| | | |

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

| (Application Serial No.) | (Filing Date) | (Status—patented, pending, abandoned) |
|---|---|---|
| (Application Serial No.) | (Filing Date) | (Status—patented, pending, abandoned) |

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent ➡

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from Semiconductor Energy Laboratory Co., Ltd. as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed ➡

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|---|---|---|
| Shunpei YAMAZAKI | Shunpei Yamazaki | 7/9/1991 |

Insert Residence Insert Citizenship ➡

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Full Name of Second Inventor, if any:

see above

| GIVEN NAME / FAMILY NAME | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| | | |

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|---|---|
| | |

| POST OFFICE ADDRESS (Complete Street Address including City, State & Country) |
|---|
| |

Full Name of Third Inventor, if any:

see above

| GIVEN NAME / FAMILY NAME | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| | | |

| RESIDENCE (City, State & Country) | CITIZENSHIP |
|---|---|
| | |

| POST OFFICE ADDRESS (Complete Street Address including City, State & Country) |
|---|
| |

Full Name of Fourth Inventor, if any:

see above

| GIVEN NAME / FAMILY NAME | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| | | |

| RESIDENCE (City, State & Country) | CITIZENSHIP |
|---|---|
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